What is claimed is:

1. A current source for use in an integrated circuit providing an extended voltage range, comprising:

a first transistor having first and second non-gate terminals;

a second transistor having first and second non-gate terminals, the first non-gate terminal coupled to the first non-gate terminal of the first transistor; and

a bias generator having a non-gate terminal coupled to the second non-gate terminals of the first and second transistors, the bias generator further having a gate terminal coupled to the first non-gate terminals of the first and second transistors.

2. The current source circuit according to claim 1, wherein the voltage range comprises a common mode range.

3. The current source circuit according to claim 1, wherein:

the second non-gate terminals of the first and second transistors comprise sources.

4. The current source circuit according to claim 1, wherein:

at least one of the first transistor, second transistor, and bias generator comprises an NMOS transistor.

5. The current source circuit according to claim 1, wherein the bias generator comprises a transistor.

6. The current source circuit according to claim 1, further comprising:

a capacitor coupled to the first non-gate terminals of the first and second transistors.

7. The current source circuit according to claim 6, wherein:

the capacitor has capacitance less than or equal to approximately 1pF.

8. The current source according to claim 6, wherein:

the capacitor has capacitance less than or equal to approximately 1fF.

9. The current source according to claim 1, wherein the first and second transistors are coupled in parallel.

10. A method of extending a voltage range of a current source for differential amplifiers and comparators in an integrated circuit, the method comprising the steps of:

providing a first transistor, a second transistor, and a third transistor, the first and second transistors each having a drain and a source, the third transistor having a gate and a drain;

connecting the drain of the first transistor to the drain of the second transistor;

connecting the source of the first transistor to the source of the second transistor;

connecting the gate of the third transistor to the drains of the first and second transistors; and

connecting the drain of the third transistor to the sources of the first and second transistors.

11. The method according to claim 10, wherein the voltage range comprises a common-mode range.

12. A current source for use in an integrated circuit providing an extended voltage range, comprising:

a voltage source;

a current source having a positive and negative terminal, wherein the positive terminal is connected to the voltage source;

a first NMOS transistor having a source terminal and drain terminal, the drain terminal connected to the negative terminal of the current source;

a second NMOS transistor having a source terminal and drain terminal, the drain terminal of the second NMOS transistor connected to the drain terminal of the first NMOS transistor, the source terminal of the second NMOS transistor connected to the source terminal of the first NMOS transistor; and

a third NMOS transistor having a gate terminal and drain terminal, the drain terminal of the third NMOS transistor connected to the source terminals of the first and second NMOS transistors, the gate terminal of the third NMOS transistor connected to the drains of the first and second NMOS transistors.

13. The current source according to claim 12, wherein the voltage range comprises a common-mode range.

14. The current source circuit according to claim 12, further comprising:

a capacitor connected to the drain terminals of the first and second NMOS transistors.

15. A current source for use in an integrated circuit providing an extended common-mode range, comprising:

means for regulating a gate-to-source voltage using a differential pair; and

coupled to the regulating means, a current driving transistor.

16. A constant current source for use in an integrated circuit extending a voltage range, comprising:

a first transistor having first and second non-gate terminals;

a second transistor having first and second non-gate terminals, the first non-gate terminal coupled to the first non-gate terminal of the first transistor;

a bias generator having a non-gate terminal coupled to the second non-gate terminals of the first and second transistors, the bias generator further having a gate terminal coupled to the first non-gate terminals of the first and second transistors; and

a fully differential receiver connected to at least one of the first non-gate terminals of the first and second transistor.

17. The current source according to claim 16, wherein the voltage range comprises a common-mode range.

18. The current source according to claim 16, wherein:

the first and second transistors are coupled in parallel.

19. A constant current source for use in an integrated circuit extending voltage range in a single ended receiver circuit, comprising:

a first transistor having first and second non-gate terminals and a gate terminal;

a second transistor having first and second non-gate terminals and a gate terminal, the first non-gate terminal of the second transistor coupled to the first non-gate terminal of the first transistor, and the gate terminal of the second transistor coupled to the gate terminal of the first transistor, the gate terminals of the first and second transistors coupled to the first non-gate terminal of the first and second transistors;

a bias generator having a non-gate terminal coupled to the second non-gate terminals of the first and second transistors, the bias generator further having a gate terminal coupled to the first non-gate terminals of the first and second transistors; and

a receiver coupled to at least one of the first non-gate terminals of the first and second transistors.

20. The current source circuit according to claim 19, wherein the voltage range comprises a common-mode range.

21. The current source circuit according to claim 19, wherein the first and second transistors are coupled in parallel.

22. A constant current source for use in an integrated circuit to extend a voltage range of a differential amplifier circuit, comprising:

a first transistor having first and second non-gate terminals;

a second transistor having first and second non-gate terminals, the first non-gate terminal coupled to the first non-gate terminal of the first transistor;

a bias generator having a non-gate terminal coupled to the second non-gate terminals of the first and second transistor, the bias generator further having a gate terminal coupled to the first non-gate terminals of the first and second transistors; and

a differential amplifier coupled to at least one of the first non-gate terminals of the first and second transistors.

23. The current source according to claim 22, wherein the voltage range comprises a common-mode range.

24. The current source circuit according to claim 22, wherein the first and second transistors are coupled in parallel.

25. A method for extending a voltage range of a current source in an integrated circuit, the method comprising the steps of:

providing a first transistor and a second transistor, the first transistor having a drain terminal and the second transistor having a gate terminal;

measuring a drain terminal voltage of the first transistor; and,

based on the drain terminal voltage, regulating a gate terminal voltage of the second transistor.

26. The method according to claim 25, wherein the voltage range comprises a common-mode range.

27. The method according to claim 25, further comprising:

a third transistor having a drain terminal;

measuring a drain terminal voltage of the third transistor; and

based on the drain terminal voltage, regulating a gate terminal voltage of the second transistor.

28. A current source for use in an integrated circuit providing an extended voltage range, comprising:

a circuit for measuring a drain voltage using a differential pair; and

a circuit for regulating a gate voltage based on the drain voltage measured at the differential pair.

29. The current source according to claim 28, wherein the voltage range comprises a common-mode range.

30. A method of extending a voltage range of a current source in an integrated circuit, the method comprising the steps of:

providing a constant current source in a saturation region of a transistor; and

maintaining the constant current if the transistor exits the saturation region.

31. The method according to claim 30 wherein the constant current is maintained by increasing the gate voltage of the transistor when the transistor leaves the saturation region.

32. The method according to claim 30, wherein the voltage range comprises a common-mode range.

33. A method for extending a voltage range of a current source in an integrated circuit, the method comprising the steps of:

measuring a drain voltage of a transistor; and

regulating a gate voltage based on the drain voltage of that transistor.

34. The method according to claim 33 wherein the gate voltage is regulated such that the current remains constant even if the transistor is not in saturation.

35. A method for extending a voltage range of a current source in an integrated circuit, the method comprising the steps of:

measuring a drain voltage using a differential pair; and

regulating a gate voltage based on the drain voltage measured at the differential pair.

36. The method according to claim 35, wherein the voltage range comprises a common-mode range.

37. A current source for use in an integrated circuit having an extended voltage range comprising:

a transistor:

having a drain characterized by a voltage; and

a gate having a voltage that is reactive to the voltage of the drain.

38. The current source according to claim 37, where the gate voltage is regulated based on the drain voltage.

39. The current source according to claim 37, wherein the gate is not directly coupled to the drain.

40. The current source according to claim 37, wherein the gate is directly coupled to the drain.

41. The current source according to claim 37, wherein the voltage range comprises a common-mode range.